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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

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APR 1 2 2002
Technology Center 2100

Complete If Known	
Application Number	10/037,861
Filing Date	January 2, 2002
First Named Inventor	Chong, Yan
Group Art Unit	2151
Examiner Name	Unassigned
Attorney Docket Number	015114-054810US

(Stamp: O I P P APR 0 8 2002 JC26 PATENT & TRADEMARK OFFICE)

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
✓	AA	5,555,214		Sung et al.	09-10-1996	
✓	AB	5,633,830		Sung et al.	05-27-1997	
✓	AC	5,764,080		Huang et al.	06-09-1998	
✓	AD	5,802,540		Sung et al.	09-01-1998	
✓	AE	5,828,229		Cliff et al.	10-27-1998	
✓	AF	5,970,255		Tran et al.	10-19-1999	
✓	AG	6,011,744		Sample et al.	01-04-2000	
✓	AH	6,049,255		Hagberg et al.	04-11-2000	
✓	AI	6,100,713		Kalb et al.	08-08-2000	
✓	AJ	6,128,692		Sung et al.	10-03-2000	
✓	AK	6,147,520		Kothandaraman et al.	11-14-2000	
✓	AL	6,236,231		Nguyen et al.	05-22-2001	
✓	AM	6,252,419		Sung et al.	06-26-2001	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
✓	AN	MICHAEL B. BENDAK et al., "CMOS VLSI Implementation of Gigabyte/Second Computer Network Links", IEEE, 1996, pp. 269-272	
✓	AO	"Virtex-II 1.5V Field-Programmable Gate Arrays", XILINX, DS031-2 (v1.5), April 2, 2001, pp. 1-38	
✓	AP	ANDREA BONI et al., "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-μm CMOS" IEEE Journal of Solid-State Circuits, vol. 36, no. 4, April 2001, pp. 706-711	
✓	AQ	"APEX II Programmable Logic Device Family", Altera Corporation, May 2001, pp. 1-8, 38-59	
✓	AR	"APEX 20K Programmable Logic Device Family", Altera Corporation, May 2001, pp. 1-8, 37-47	

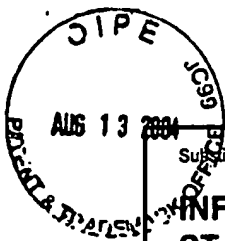| Examiner Signature	Examiner signature	Date Considered	7/13/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

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Examiner Name	Thomas C. Lee
Attorney Docket Number	015114-054810US

U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No.[1]	Document Number — Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
✓	AA	US-6,279,073	08-21-2001	McCracken et al.	RECEIVED
✓	AB	US-6,472,904	10-29-2002	Andrews et al.	
✓	AC	US-6,504,790	01-07-2003	Wolford	AUG 1 8 2004
✓	AD	US-			
/	AE	US-			Technology Center 2100

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Examiner Initials*	Cite No.[1]	Foreign Patent Document — Country Code[3]	Number[4]	Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	AF							☐
	AG							☐

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	AH		
	AI		
	AJ		

Examiner Signature	*Vani*	Date Considered	7/13/05